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Digital Electronics II Solutions 2013 Page 1 of 8 2013 Paper E2.1: Digital Electronics II- Solutions (With annotations) 1. (a) This question tests student's ability to analyse a simple state machine. It is helpful to draw the transition table first: Q2#Q1#Q0##Next_Q2#Next_Q1#Next_Q0#(D)#

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1. (a) Figure 1.1 shows a circuit with two D flip-flops FF1 and FF2 with setup and hold times of 2 ns and 1 ns respectively, and a clock-to-Q output delay of 2 ns. The clock signal CLK has a 1:1 mark-space ratio. The signal path has two combinational circuits, LUT_1 and LUT_2, each having a propagation delay between 1 ns and 5 ns.

2018 Paper E2.1: Digital Electronics II

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